REMARKS

The Office Action rejected claims 27, 28, 32, 46, and 47 under 35 U.S.C. §102(e) as being anticipated by the United States Patent 6,798,421 issued to Baldwin ("Baldwin"). The Office Action rejected claims 1 and 34 under 35 U.S.C. §103(a) as being unpatentable over Baldwin in view of the United States Patent 6,738,895 issued to Klein ("Klein"). The Office Action also rejected claims 2, 23, and 35 under §103(a) as being unpatentable over Baldwin and Klein in view of the United States Patent 6,958,757 issued to Karlov ("Karlov"). The Office Action also rejected claims 4, 5, 8, and 24 under §103(a) as being unpatentable over Baldwin, the United States Patent 6,269,390 issued to Boland ("Boland"), and the United States Patent 6,470,443 issued to Emer, et al. ("Emer"). The Office Action also rejected claims 6 and 25 under §103(a) as being unpatentable over Baldwin, Boland, and Emer in view of Karlov. The Office Action also rejected claims 10, 11, 14, 37, 38, 41, 50, and 51 under §103(a) as being unpatentable over Boland and Emer. The Office Action also rejected claims 13, 21, and 40 under §103(a) as being unpatentable over Boland and Emer in view of the United States Patent 4,876,651 issued to Dawson, et al. ("Dawson"). The Office Action also rejected claims 15, 17, 18, 22, 42, and 44 under §103(a) as being unpatentable over Boland and Emer in view of the United States Patent 6,995,770 issued to Ngai ("Ngai"). The Office Action also rejected claim 20 under §103(a) as being unpatentable over Boland and Emer in view of the United States Patent 5,657,478 issued to Recker, et al. ("Recker"). The Office Action also rejected claims 26 and 45 under §103(a) as being unpatentable over Baldwin and the United States Patent 6,933,945 issued to Emberling ("Emberling"). The Office Action also rejected claims 29, 31, 33, and 49 under §103(a) as being unpatentable over Baldwin in view of Karlov. Furthermore, the Examiner objected to claims 3, 7, 30, 36 and 48 as being dependent upon a rejected based claim. However, the Examiner stated that claims 3, 7, 30, 36, and 48 would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

In this Response, Applicants have not added, amended, or canceled any claims. Accordingly, claims 1-8, 10-11, 13-15, 17-18, 20-38, 40-42, and 44-51 will be pending after entry of this Response.

I. Rejection to Claims 1, 2, 23, 34, and 35

The Office Action rejected claims 1 and 34 under §103(a) as being unpatentable over Baldwin in view of Klein. The Office Action also rejected claims 2, 23, and 35 under §103(a) as being unpatentable over Baldwin and Klein in view of Karlov.

Claims 2 and 23 are directly or indirectly dependent on claim 1. Claim 1 recites a method of executing a set of at least two image processing routines on a processor using a particular cache. Each routine in the set of routines processes at least one source, which is a frame of video data. The method determines a size of a band based on the size of the particular cache. The source is divisible into two or more bands. The method executes the set of routines in two or more passes. During each pass, the routine processes at least one band from the particular cache and produces output data stored to the particular cache. The execution of the passes is performed using the particular cache without accessing other memories.

Applicants respectfully submit that Baldwin, Klein, or their combination does not render claim 1 unpatentable for at least the following reasons. *First*, Applicants respectfully submit that Baldwin, Klein, or their combination does not render obvious determining a size of a band based on a size of the particular cache. The Office Action cites column 18, lines 46-59 and column 5, lines 21-31 of Baldwin to suggest such a limitation. Specifically, the Office Action cites to a tile within Baldwin to suggest a band. *See*, Office Action, page 5 ("determining size of band (tile)").

Applicants respectfully submit that Baldwin does not disclose or suggest that the size of a tile (i.e., the alleged band) is determined based on the size of the particular cache. Baldwin recites that "[a] tile is an 8x8 square of pixels and is always screen aligned on 8 pixel boundaries." *See*, Baldwin, column 4, lines 63-64. The cited lines only state that the cache is of a particular size and that a number of tiles may be held within the cache. *See*, Baldwin, column 18, lines 46-48. The reference does not disclose or suggest that the size of a tile (i.e., the alleged tile) is determined by the size of the cache.

Moreover, the reference states that routines are executed on each tile not on a number of tiles. *See*, Baldwin, column 18, lines 20-23 ("Each Tile message has an extra filed to indicate which tile program (first, middle or last) to run…"). Consequently, the reference does not disclose or suggest that a number of tiles equates to a band over which a routine is executed. Accordingly, Baldwin does not disclose or suggest the second limitation of claim 1 that recites executing a set of routines in at least two passes where a pass includes each routine processing a single band. Accordingly, Applicants respectfully submit that Baldwin, Klein, or their combination does not render obvious determining a size of a band based on a size of the particular cache.

Second, Applicants respectfully submit that Baldwin, Klein, or their combination does not render obvious executing a set of routines where each routine processes a single band retrieved from the particular cache to produce output data stored to the particular cache and where executing of the passes is performed using the particular cache without accessing other memories outside the processor. The Office Action states that Baldwin does not teach such a limitation. *See*, Office Action page 6. However, the Office Action cites column 6, lines 24-30 of Klein stating that "Klein teaches being able to directly read and write data from/to cache without registers." *See*, Office Action page 6.

Applicants respectfully submit that, in the cited lines, Klein recites caching program instructions. *See*, Klein, column 6, lines 20-24. Klein does not disclose caching the operands processed by the instructions (e.g., bands processed by a routine) or the output produced by the instructions. *See*, Klein, figure 2 step 222. Consequently, Applicants respectfully submit that Baldwin, Klein, or their combination does not render obvious executing a set of routines where each routine processes a single band retrieved from the particular cache to produce output data stored to the particular cache and where executing of the passes is performed using the particular cache without accessing other memories outside the processor.

In view of the foregoing remarks, Applicants respectfully submit that Baldwin does not render claim 1 invalid. Given that claims 2 and 23 are dependent on claim 1, Applicants respectfully submit that these claims be allowable over the cited reference for at least the same reasons that were provided above for claim 1. Accordingly, Applicants respectfully request reconsideration and withdrawal of the §103(a) rejections to claims 1, 2, and 23.

Furthermore, claim 34 was rejected along the same rationale as claim 1. Accordingly, claim 34 is patentable over the references because the references do not render obvious determining a size of a band based on a size of the particular cache, as argued above for claim 1. Also, claim 34 is patentable over the references because the references do not render obvious executing a set of routines where each routine processes a single band retrieved from the particular cache to produce output data stored to the particular cache and where executing of the passes is performed using the particular cache without accessing other memories outside the processor, as argued above for claim 1. Given that claim 35 is dependent on claim 34, Applicants respectfully submit that this claim be allowable over the cited references for at least the same reasons that were provided above for claims 1 and 34. Therefore, Applicants respectfully submit that the cited references do not render claims 34 and 35 invalid. Applicants respectfully request reconsideration and withdrawal of the rejections to claims 34 and 35.

II. Rejection to Claims 4-6, 8, 24, and 25

The Office Action rejected claims 4, 5, 8, and 24 under §103(a) as being unpatentable over Baldwin, Boland, and Emer. The Office Action also rejected claims 6 and 25 under §103(a) as being unpatentable over Baldwin, Boland, and Emer in view of Karlov.

Claims 5, 6, 8, 24, and 25 are directly or indirectly dependent on claim 4. Claim 4 recites a method of processing a group of image processing routines on a processor by using a cache. Each routine in the group of routines processes at least one frame of video data. The method determines an initial list of routine identifiers positioned in a specific order which when executed according to the specific order produce a particular effect. The group of routine identifiers identifies the group of image processing routines, where each routine identifier identifies a corresponding routine in the group of routines. The method groups two or more routine identifiers and modifies the initial list of routine identifiers to indicate the grouping of the at least two routine identifiers to produce a modified ordering of the initial list of routine identifiers. The grouping of routine identifiers and the modification of the initial list are performed by a set of instructions executed by the processor. The method executes the routines identified in the modified ordering of routine identifiers by traversing the modified list of routine identifiers to produce the particular effect. The method then stores the output of the routines to a computer-readable medium.

Applicants respectfully submit that Baldwin, Boland, and Emer, or their combination does not render obvious the method of claim 4 for at least the following reasons. *First*, Applicants respectfully submit that these references do not render obvious a method of processing image processing routines on a processor where the method includes (1) determining an initial list of routine identifiers, (2) grouping at least two routine identifiers, (3) modifying the initial list of routine identifiers, (4) executing the routines in the modified list, and (5) storing output of the routines. The Office Action states that Baldwin teaches processing image processing routines on a processor, but that Baldwin does not teach the determining, grouping, modifying, executing, and storing limitations. To suggest these limitations, the Office Action cites Boland stating that it would have been obvious to one of ordinary skill in the art at time of invention to modify Baldwin to incorporate the teachings of Boland. *See*, Office Action, page 9.

However, Applicants respectfully submit that Boland teaches away from Baldwin's suggested teachings for the processing of image processing routines on a processor. Specifically, Boland teaches away from using a processor. Instead, Boland relates "to multiprocessing systems and, more particularly, to a method for scheduling the execution of processes among processors within a multiprocessing system…". *See*, Boland, column 1, lines 4-6 (emphasis added) and column 2, lines 45-49. Accordingly, any combination of these references results in a multi-processor method or system as opposed to the method of claim 4 reciting a method of processing image processing routines on a processor where the method includes (1) determining an initial list of routine identifiers, (2) grouping at least two routine identifiers, (3) modifying the initial list of routine identifiers, (4) executing the routines in the modified list, and (5) storing output of the routines.

Second, Applicants respectfully submit that there are no motivations or suggestions to combine (1) the alleged teachings of Baldwin for processing image processing routines on a processor using a cache, (2) the alleged teachings of Boland for determining, grouping, modifying, executing, and storing, and (3) the alleged teachings of Emer for using routine identifiers. As the US Supreme Court has affirmed, "a patent composed of several elements is not proved merely by demonstrating that each of its elements was, independently, known in the prior art… it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant filed to combine the elements in the way the claimed new invention does." *KSR Int'l Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396, 127 S. Ct. 1727, 1741 (U.S. 2007). Here, the Examiner has effectively asserted that the claim is obvious because each of its elements was independently known in the prior art, but has not provided a valid reason why it would be obvious to combine the references. Furthermore, this reason would have to be obvious at the time of filing of the application.

Moreover, 35 U.S.C. §103 requires that "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made…". *See also*, MPEP §2141.02 ("the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious"). Applicants respectfully submit that the piecemeal combination of three separate references for three separate aspects of the claimed limitations of claim 4 used in the Office Action fails to establish a proper § 103(a) rejection. Without using the Applicants' invention as a roadmap, it would not have been obvious to combine Baldwin, Boland, and Emer. Accordingly, Applicant respectfully submits that a case of obviousness for rejecting claim 4 has not been established.

In view of the foregoing remarks, Applicants respectfully submit that the cited references do not render claim 4 invalid. Given that claims 5-6, 8, 24, and 25 are directly or indirectly dependent on claim 4, Applicants respectfully submit that these claims be allowable over the cited references for at least the same reasons that were provided above for claim 4. Accordingly, Applicants respectfully request reconsideration and withdrawal of the §103(a) rejection of claims 4-6, 8, 24, and 25.

III. Rejection to Claims 10, 11, 13, 37, 38, and 40

The Office Action rejected claims 10, 11, 37, and 38 under §103(a) as being unpatentable over Boland and Emer. The Office Action also rejected claims 13 and 40 under §103(a) as being unpatentable over Boland and Emer in view of Dawson.

Claims 11 and 13 are directly or indirectly dependent on claim 10. Claim 10 recites a method of processing a group of routines. The method determines an initial list of routine identifiers that identify the group of routines where executing the initial list of routine identifiers produces a particular effect. Each routine identifier identifies a corresponding routine in the group of routines. The method identifies a set of at least two routine identifiers in the initial list of routine identifiers that are combinable into a single routine. The single routine is capable of performing each routine in the set of routines. Each routine includes a group of instructions. The method determines a single routine identifier that identifies the single routine and that produces the particular effect when executed with the other routine identifiers that were not identified as combinable into the single routine identifier. The identification of the combinable routine identifiers and the determination of the single routine identifier are performed by an automated set of instructions executed by the processor. The method stores the single routine identifier to a computer-readable medium.

Applicants respectfully submit that Boland, Emer, or their combination does not render obvious the method of claim 10 for at least the following reason. Applicants respectfully submit that these references do not render obvious determining a single routine identifier that identifies the single routine that identifies a set of at least two routine identifier. The Office Action states that Boland does not teach determining a single routine identifiers. However, the Office Action cites column 1, lines 18-25, column 4, lines 1-10, and column 4, lines 60-63 of Emer to suggest such a limitation. *See*, Office Action, pages 13-14.

Applicants respectfully submit that the cited lines of Emer also do not disclose or suggest determining a single routine identifier for a single routine that identifies a set of at least two routine identifiers. Specifically, column 1, lines 18-25 of Emer recites an out-of-order execution CPU without disclosing or suggesting a single routine identifier for the single routine that identifies a set of at least two routine identifiers. The Office Action then states that column 4, lines 1-10 of Emer suggests fetching and merging multiple instructions into a single instruction/routine. However, Applicants respectfully submit that Emer does not disclose or suggest determining a single routine identifier for the merged instructions. Moreover, neither column 4, lines 9-10 of Emer nor column 4, lines 60-63 suggests determining a single routine identifier for a single routine that identifies a set of at least two routine identifiers. Specifically, column 4, lines 9-10 provides an identifier for each instruction rather than the combined set of instructions. Column 4, lines 60-63 of Emer suggests combining the instructions into an instruction queue rather than determining a single routine identifier for a single routine that identifies a set of at least two routine identifier. Accordingly, Applicants respectfully submit that these references do not render obvious determining a single routine identifier that identifies the single routine that identifies a set of at least two routine identifiers.

In view of the foregoing remarks, Applicants respectfully submit that Boland, Emer, or their combination does not render claim 10 invalid. Given that claims 11 and 13 are dependent on claim 10, Applicants respectfully submit that these claims be allowable over the cited reference for at least the same reasons that were provided above for claim 10.

Furthermore, claim 37 was rejected along the same rationale as claim 10. Accordingly, claim 37 is patentable over Boland, Emer and their combination, because the references do not render obvious determining a single routine identifier that identifies the single routine that identifies a set of at least two routine identifiers. Given that claim 38 is dependent on claim 37, Applicants respectfully submit that claim 38 is patentable over the references for the reasons given above for claims 10 and 37. Therefore, Applicants respectfully submit that the cited references do not render claims 37 and 38 invalid. Applicants respectfully request reconsideration and withdrawal of the §103(a) rejections to claims 10, 11, 13, 37, and 38.

IV. Rejection to Claims 14, 15, 17, 18, 20-22, 41, 42, 44, 50 and 51

The Office Action rejected claims 14, 41, 50, and 51 under §103(a) as being unpatentable over Boland and Emer. The Office Action also rejected claim 21 under §103(a) as being unpatentable over Boland and Emer in view of Dawson. The Office Action also rejected claims 15, 17, 18, 22, 42, and 44 under §103(a) as being unpatentable over Boland and Emer in view of Ngai. The Office Action also rejected claim 20 under §103(a) as being unpatentable over Boland and Emer in view of Recker.

Claims 15, 17, 18, 20-22, and 50 are directly or indirectly dependent on claim 14. Claim 14 recites a method of executing a group of routines for processing by at least one processor. The method determines an initial list of routine identifiers that identify the group of routines which when executed produce a particular effect. Each routine identifier identifies a corresponding routine. The method identifies at least two routine identifiers in the initial list of routine identifiers as sendable routine identifiers, each sendable routine identifier identifying a sendable routine which may be processed by a second processor. Before executing the routines identified in the list of routine identifiers, the method modifies the list of routine identifiers by grouping the sendable routine identifiers into at least one set of successive sendable routine identifiers. The grouping reduces the number of data transfers between the first and second processors. The identification of the sendable routine and the modification of the list of routine identifiers are performed by an automated set of instructions executed by the processor. The method stores the modified list of routine identifiers to a computer-readable medium.

Applicants respectfully submit that Boland, Emer, or their combination does not render obvious determining an initial list that includes routine identifiers identifying several routines which when executed produce a particular effect. The Office Action cited to column 3, lines 61-67 of Boland to suggest such a limitation. The cited lines recite a scheduler that "schedules all runnable processes in global run queue 24, including new processes as well as processed which have been previously run and are now affinitized to a specific processor" (emphasis added). Accordingly, the scheduling provided by Boland does not pertain to producing a particular effect, but rather to scheduling any general process in a multi-processor system. Accordingly, Applicants respectfully submit that the cited lines do not disclose determining an initial list that includes routine identifiers identifying several routines which when executed produce a particular effect.

In view of the foregoing remarks, Applicants respectfully submit that the cited references do not render claim 14 invalid. Given that claims 15, 17, 18, 20-22, and 50 are dependent directly or indirectly on claim 14, Applicants respectfully submit that these claims be allowable over the cited references for at least the same reasons that were provided above for claim 14. Accordingly, Applicants respectfully request reconsideration and withdrawal of the §103(a) rejection of claims 14, 15, 17, 18, 20-22, and 50.

Furthermore, claim 41 was rejected along the same rationale as claim 14. Accordingly, claim 41 is patentable over Boland, Emer, and their combination, because the references do not render obvious determining an initial list that includes routine identifiers identifying several routines which when executed produce a particular effect. Given that claims 42, 44, and 51 are dependent directly or indirectly on claim 41, Applicants respectfully submit that these claims be allowable over the cited references for at least the same reasons that were provided above for claims 14 and 41. Applicants respectfully request reconsideration and withdrawal of the §103(a) rejections to claims 41, 42, 44, and 51.

V. Rejection to Claims 26 and 45

The Office Action rejected claims 26 and 45 under §103(a) as being unpatentable over Baldwin and Emberling. Claim 26 recites a method of executing a set of at least two image processing routines on a processor using a particular cache. Each routine in the set of routines processes at least a frame of video data. The method determines a size of a band of a frame of vide data based on a size of the particular cache and a number of buffers referenced by the routine. The frame of video data is divisible into at least two bands. The method executes the set of routines in two or more passes. During each pass, the routine processes at least one band from the particular cache and produces output data stored to the particular cache.

Applicants respectfully submit that Baldwin, Emberling, or their combination does not render claim 26 unpatentable for at least the following reasons. *First*, Applicants respectfully submit that Baldwin, Emberling, or their combination does not render obvious determining a size of a band based on a size of the particular cache and a number of buffers referenced by the routine. The Office Action states Baldwin does not teach determining the size of a band based on buffers referenced by a routine. However, the Office Action cites column 15, lines 20-32 and 50-58 of Emberling to suggest such a limitation.

Applicants respectfully submit that the cited lines of Emberling disclose a filtering unit, bit scanline memories, and a bit cache array. The cited lines do not disclose a routine or the determining of a size of a band based on a size of the particular cache and a number of buffers referenced by the routine.

Second, Applicants respectfully submit that Baldwin, Emberling, or their combination does not render obvious executing a set of routines where each routine processes a single band retrieved from the particular cache to produce output data stored to the particular cache.

The Office Action cites column 18, lines 5-35 of Baldwin to suggest the processing a single band retrieved from a particular cache to produce output data stored to the same particular cache. However, Baldwin specifies executing its operations using two separate memories instead of executing the operations using a single cache (i.e., memory) as recited in claim 26. Baldwin recites (1) initially retrieving data from a Pixel Cache and (2) processing the data and writing the processed data to a SIMD memory element of a Pixel Unit. *See*, Baldwin, column 18, lines 5 and 23-25. Accordingly, Baldwin does not disclose or even suggest processing a single band retrieved from a particular cache to produce output data stored to the same particular cache

Specifically, Figure 1B of Baldwin illustrates the Pixel Unit and Pixel Cache as two separate elements with the description of each element specifying that each element includes a memory (e.g., the Pixel Unit having SIMD memory elements and the Pixel Cache storing pixel data). *See*, Baldwin, column 17, lines 59-60 and column 18, lines 5-7. Baldwin recites the Pixel Unit retrieving pixel data from the Pixel Cache. *See*, Baldwin, column 18, lines 5-7. Baldwin then states that "any data to be carried over from one pass to the next is held in the local register file present in each SIMD element." *See*, Baldwin, column 18, lines 23-25 (emphasis added). As such, Baldwin retrieves data from a first memory (i.e., the Pixel Cache) and writes output data to a second memory (i.e., SIMD element of the Pixel Unit). Therefore, Applicants respectfully submit that Baldwin does not disclose or even suggest processing a single band retrieved from a particular cache to produce output data stored to the same particular cache.

In view of the foregoing remarks, Applicants respectfully submit that Baldwin does not render claim 26 invalid. Furthermore, claim 45 was rejected along the same rationale as claim 26. Accordingly, claim 45 is patentable over Baldwin, Emberling, or their combination because the references do not render obvious determining a size of a band based on a size of the particular cache and a number of buffers referenced by the routine, as argued above for claim 26. Claim 45 is also patentable over Baldwin, Emberling, or their combination because the references do not render obvious executing a set of routines where each routine processes a single band retrieved from the particular cache to produce output data stored to the particular cache, as argued above for claim 26. Therefore, Applicants respectfully submit that the cited references do not render claims 26 and 45 invalid. Applicants respectfully request reconsideration and withdrawal of the rejections to claims 26 and 45.

VI. Rejection to Claims 27-29, 31-33, 46-47, and 49

The Office Action rejected claims 27, 28, 32, 46, and 47 under 35 U.S.C. §102(e) as being anticipated by Baldwin. The Office Action also rejected claims 29, 31, 33, and 49 under §103(a) as being unpatentable over Baldwin in view of Karlov.

Claims 28, 29, and 31-33 are directly or indirectly dependent on claim 27. Claim 27 recites a method of executing a set of at least two image processing routines on a processor using a particular cache. Each routine in the set of routines processes at least a frame of video data. The method determines a size of a band of a frame of video data. The frame of video data is divisible into two or more bands. The method executes the set of routines in two or more passes. During each pass, the routine processes several bands referenced by the routine and retrieved from the particular cache in order to produce output data stored to the particular cache.

Applicants respectfully submit that Baldwin does not render claim 27 unpatentable for at least the following reason. Applicants respectfully submit that Baldwin does not disclose or suggest executing a set of routines where each routine processes several bands referenced by a routine and retrieved from the particular cache in order to produce output data stored to the particular cache. The Office Action cites column 18, lines 5-35 of Baldwin to suggest such a limitation. However, Baldwin specifies executing its operations using two separate memories instead of executing the operations using a single cache (i.e., memory) as recited in claim 27. Baldwin recites (1) initially retrieving data from a Pixel Cache and (2) processing the data and writing the processed data to a SIMD memory element of a Pixel Unit. *See*, Baldwin, column 18, lines 5 and 23-25. Accordingly, Baldwin does not disclose or suggest executing a set of routines where each routine processes several bands referenced by a routine and retrieved from the particular cache in order to produce output data stored to the particular cache.

Specifically, Figure 1B of Baldwin illustrates the Pixel Unit and Pixel Cache as two separate elements with the description of each element specifying that each element includes a memory (e.g., the Pixel Unit having SIMD memory elements and the Pixel Cache storing pixel data). *See*, Baldwin, column 17, lines 59-60 and column 18, lines 5-7. Baldwin recites the Pixel Unit retrieving pixel data from the Pixel Cache. *See*, Baldwin, column 18, lines 5-7. Baldwin then states that "any data to be carried over from one pass to the next is held in the local register file present in each SIMD element." *See*, Baldwin, column 18, lines 23-25 (emphasis added). As such, Baldwin retrieves data from a first memory (i.e., the Pixel Cache) and writes output data to a second memory (i.e., SIMD element of the Pixel Unit). Therefore, Applicants respectfully submit that Baldwin does not disclose or even suggest executing a set of routines where each routine processes several bands referenced by a routine and retrieved from the particular cache in order to produce output data stored to the particular cache.

In view of the foregoing remarks, Applicants respectfully submit that Baldwin does not render claim 27 invalid. Given that claims 28, 29, and 31-33 are dependent on claim 27, Applicants respectfully submit that these claims be allowable over the cited reference for at least the same reasons that were provided above for claim 27. Accordingly, Applicants respectfully request reconsideration and withdrawal of the §102(e) rejections to claims 27-29 and 31-33.

Furthermore, claim 46 was rejected along the same rationale as claim 27. Accordingly, claim 27 is patentable over Baldwin because Baldwin does not disclose or suggest executing a set of routines where each routine processes several bands referenced by a routine and retrieved from the particular cache in order to produce output data stored to the particular cache, as argued above for claim 27. Given that claims 47 and 49 are dependent on claim 49, Applicants respectfully submit that these claims be allowable over the cited reference for at least the same reasons that were provided above for claims 27 and 46. Therefore, Applicants respectfully submit that the cited reference does not render claims 46, 47, and 49 invalid. Applicants respectfully request reconsideration and withdrawal of the rejections to claims 46, 47, and 49.

VII. Allowable Claims 3, 7, 30, 36 and 48

In the Office Action, the Examiner objected to claims 3, 7, 30, 36, and 48 as being dependent upon a rejected base claim. The Examiner stated that claims 3, 7, 30, 36, and 48 were otherwise allowable if rewritten in independent form. Applicants respectfully thank the Examiner for the allowance. However, Applicants respectfully have not rewritten any of these claims in independent form since Applicants respectfully believe that the rejected independent claims for claims 3, 7, 30, 36, and 48 are patentable over the cited references.

CONCLUSION

In view of the foregoing, it is submitted that all pending claims, namely claims 1-8, 10-11, 13-15, 17-18, 20-38, 40-42, and 44-51 are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Applicants have submitted all known required fees. Applicants believe that no additional fee is required for the submission of this Response. However, in the unlikely event that the Commissioner determines that additional fees, extensions of time, and/or other relief are required, Applicants petition for any required relief. Moreover, Applicants authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. **50-3804** referencing **APLE.P0063**.

Should there remain unresolved issues that require adverse action, Applicants respectfully request that the Examiner telephone the below signed attorney or agent so that such issues may be resolved as expeditiously as possible.

Respectfully submitted,

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